REMARKS

Claims 1-18 are pending. Claims 6-11 have been withdrawn from consideration. Reconsideration and allowance in view of the following remarks are respectfully requested.

The Office rejects claims 1, 13, 14, 16 and 17 under 35 U.S.C. §103(a) as being unpatentable over Kuroda (US 5,487,029) in view of Clemons, (US 4,599,709); claims 2-5 under 35 U.S.C. §103(a) as being unpatentable over Clemons, Kuroda and Dierke; and claims 12, 15 and 18 under 35 U.S.C. §103(a) as being unpatentable over Kuroda, Clemons and Seyyedy (US 5,969,380). These rejections are respectfully traversed.

For reasons of brevity applicants' previous remarks filed on December 27, 2006 and July 23, 2007 are hereby incorporated by reference.

Applicants respectfully submit that it appears that the Examiner doesn't fully appreciate the present invention and also appears to partly misunderstand or interpret the prior art. In this regard, applicants provide the following comments directed to providing an accurate understanding of the embodiments of the present invention as well as the prior art and the inability to combine teachings directed to very different memory types as disclosed in the cited prior art.

Embodiments of the Present Invention

The present invention concerns a passive matrix-addressable ferroelectric or electret memory. This of course follows from the fact that the memory is an electrically polarizable dielectric material exhibiting hysteresis. Moreover the memory device according to the invention is a passive device, i.e. all the memory cells of the memory array is contacting the electrodes permanently. This contrasts with an active matrix-addressable memory, wherein each memory cell comprises a switching means, usually a FET transistor for establishing an electrical circuit between the memory cells and for instance its bit line electrode. This means that while all the memory cells of a passive matrix-addressable memory permanently are connected in an RC

network, in an active matrix-addressable memory a memory cell selected for an addressing operation, i.e. a write or read operation, is switched into the network by switching means connected with a memory cell.

Both types of memory have their advantages and disadvantages. In a passive matrix-addressable memory a write or read operation consists in applying a switching voltage or potential over a selected memory cell and record a charge or current output response on the bit line by means a sense amplifier connected thereto. The so-called switching voltage which is applied for an addressing operation is usually selected much larger than their coercive voltage of the memory material, and this implies that as an average a memory cell will be switched in 50% of the addressing operations, i.e. its polarization direction will be reversed. This amounts to a destruction of the datum stored in the memory cell, such that for instance a stored logical 0 will be switched to a logical 1. In such cases a memory cell has to be reset by performing a writing operation and this is done by once more applying a switching voltage to the memory cell, but of the opposite sign. In a passive matrix-addressable memory an addressing scheme with destructive write and read sets up so-called sneak currents and disturb voltages in the permanent RC network formed by the memory cells of the array. This in addition to parasitic or stray capacitances that are bound to occur, and in sum these effects may either change the set polarization state of a memory cell and cause spurious output responses on the bit lines in a read operation.

As well known to persons skilled in the art the unfortunate effects of destructive write and read in a passive matrix addressable array is abated by for instance subjecting all addressing operations to a so-called voltage pulse protocol and the use of an appropriate voltage selection rule which will serve to minimize potential differences on unselected memory cells during an addressing operation.

The unfortunate effects in connection with the destructive write and read operation are avoided in active matrix-addressable memories, since only a selected memory cell is connected to a word line and a bit line. Usually such memory cells are termed 1T-1C memory cell, which

denotes a memory cell with one switching transistor and one ferroelectric capacitor (for instance). Other configurations are known, e.g. memory cells of the type 2T-2C etc. The penalty of this is that the use of switching transistors in an active matrix tends to be power-consuming and moreover makes the memory array larger and more complicated. Also the number of electrode lines is doubled, as selection lines for the gate electrodes of the switching transistors will bee needed and the data has to be output on a data line, which is joined to one memory cell electrode. i.e. one of the plates of the capacitor formed by the memory cell, upon switching the transistor channel to conduction. The data line is then for instance connected to the drain contact of the switching transistor. The bit line proper is then the electrode that connects one or more e.g. ferroelectric capacitors with the source contact of the switching transistor. It should furthermore be noted that even an active matrix-addressable array is not completely free from parasitic capacitances, which by the way is a well-known problem in integrated circuit technology.

Generally ferroelectric memories have a much slower response than semiconductor memories such as DRAMs and SRAMs and hence the ferroelectric memories are better suited for use as ROM and WORM (Write Once, Read Many times). It should also be noted that in ferroelectric memories the data content cannot be erased, i.e. the memory cannot be set to a virgin state, but is non-volatile in the sense that a polarization state in principle could be maintained indefinitely and only completely erased by raising the temperature of the memory above the Curie temperature of the ferroelectric material, something which will return the material to its paraelectric phase. However, the fairly slow response of a ferroelectric memory can be offset by reading a large number of memory cells in parallel. In principle all memory cells on a word line can be read simultaneously, provided that each bit line is connected with a sense amplifier. Now there is also a penalty for this. While e.g. ferroelectric memory arrays can be made extremely large, comprising millions or even hundred of millions of memory cells, it has turned out that it is difficult to operate a memory with more that 2000 word lines. In that case each bit line will be permanently connected in the passive configuration to no more than 2000 memory cells. One reason for this is the occurrence of floating charges on the bit line, a problem that aggravates with the number of memory cells on the bit line, and while it could be tempting to lower the access rate so that floating charges may decay, this would make the memory

intolerably slow to operate. So the number of word lines is for practical reasons the typical ferroelectric memory material limited to about 2000, the exact number being dependent on the actual ferroelectric memory material used.

The capacity of memory can, however, be increased by resorting to a large number of bit lines, e.g. 16000 or 32000, which would respectively produce a memory array of 32 or 64 million memory cells. Performing a parallel readout of all memory cells on a word line in the latter case would imply that each bit line is connected with a sense amplifier, making 32000 sense amplifiers all told. It is easily seen that this would even with a slow response time of 1 μs yield a data rate corresponding to 32 GHz. There are several reasons why this arrangement is not desirable. One is the problem of handling this data rate, the other is the very large number of sense amplifiers that is needed, and considering that a sense amplifier usually comprises two operation amplifiers, this implies at least 50 to 60 transistors for each sense amplifier. However, a more than adequate data rate would be 1 GHz, which would be competitive with fast DRAMs and SRAMs and would then, of course, imply parallel read of 1000 bit lines at once. Typically a data word read in this manner shall consist of 1 K bits or 128 bytes. By dividing the word line into segments of say 1024 memory cells a correspondingly large data word may be read in about 1 μs by connecting all the bit lines forming the word line segment to sense amplifiers. As a consequence a number of sense amplifiers can be reduced to the number of bit lines in a word line segment and with obvious advantages. This is precisely what the present invention discloses. Such an arrangement is not known in the prior art, and is neither anticipated nor suggested in any or the prior art documents cited by the Examiner.

Prior Art References

Kuroda

Kuroda, which appears to be the main citation, is not concerned with a true passive matrix-addressable ferroelectric memory, and attempts to solve a completely different problem than the present invention. Kuroda discloses a block-segmented ferroelectric memory which in

preferred embodiments comprises 16 memory blocks of 64 memory cells each, the blocks being arranged in an array with 8 blocks to a row and 2 blocks to a column. The object of Kuroda is specifically to obtain a combination of the best of both worlds, namely the simplicity of a passive matrix-addressable ferroelectric memory with the disturb immunity of active matrix-addressable ferroelectric memory. To this end Kuroda provides means for selecting a single memory block at a time, and then selecting a memory circuit comprising 8 memory cells in a block sharing a bit line that is switched to contact with an output data line by means of an active word line, actually a gating electrode line.

For each memory cell it is furthermore provided a word line which appears to be through-going in a row of blocks thus connecting 64 memory cells. In this manner Kuroda is able, as he intends, to reduce the number of switching transistors to 1 for each memory circuit of 8 memory cells, thus requiring only 128 switching transistors in memory blocks of a preferred embodiment of his memory device. This implies that on addressing and selecting a specific memory cell at most the 7 other memory cells of the memory circuit will be subjected to a voltage disturb, and this problem Kuroda proposes to handle by applying a voltage pulse protocol employing a so-called half-selection rule, i.e. one using the voltage levels 0, ½ V_S and V_S in the addressing scheme.

Specifically the advantages achieved with Kuroda's particular configuration are discussed in connection with Table 1 in cols. 16 and 17, and further discussed in col. 17, and up to line 13 in col. 18. However, it should be noted that for each column Kuroda needs a multiplexer arrangement for selecting and connecting the appropriate data line to a write/read output device comprising a read sense amplifier SA and a write amplifier WA in a column of memory blocks. Kuroda is now able to select at most one memory cell in each block for an addressing operation. On the other hand in this peculiar configuration the Kuroda memory device also allows the simultaneous selection of a single memory cell on the same word line in each of the 7 other memory blocks sharing this word line. In other words, Kuroda is able to at most output 8 bits in parallel and similarly also be able to write 8 bits in parallel. In a bytewise-organized memory this has the disadvantage that a data word must be distributed willy-nilly among the 8 memory blocks

in a row, leading to more complicated addressing and switching schemes for storing and reading data in terms of a bytewise organization.

Clemons

Clemons, which has been cited in conjunction with Kuroda, concerns a completely different kind of memory, namely a semiconductor memory of the SRAM type and a multi-bit organization. Clemons discloses how to achieve a memory architecture tailored to a bytewise organization by dividing the memory into block-like arrangement such that all bits of a byte accessed in a given operation are obtained from physically adjacent columns referred as byte blocks and thus distinguished above input/output blocks in prior art, see Clemons col. 4, lines 40-45. So generally Clemons teaches nothing than providing a bytewise-organized memory by defining blocks of the memory in terms of a bytewise arrangement made up of adjacent data lines such that, for instance, a byte may be read in parallel from one row of memory cells in a block at a time.

Since Clemons is not at all concerned with ferroelectric or electret memories, but rather a semiconductor SRAM memory, it is a dubious claim that his teaching can be hoisted on Kuroda. The teaching of Clemons would actually ruin the expressed object of Kuroda as it would demand that all 8 memory circuits of a block in Kuroda's memory should be selected and connected, for example, a write or read operation. This would increase the voltage stress ratio of Kuroda's memory eight-fold, but in addition it would also serve to make Kuroda's memory rather more complicated as it would need a complete rearrangement of the Y-Select block as well as the Write/Read Control Block(WRC). The latter must for instance be equipped with 8 sense amplifiers, but even this would not transform Kuroda's device into one similar of the present invention, with regard to operational features, as further multiplexing arrangements would be needed if for instance the Write/Read Control Blocks were to be conflated into one and used for all columns of this memory. However, it is quite clear that at least what could be termed multiplexing arrangement of Clemons cannot be adapted to a memory of Kuroda in that sense, even when the fact that they are completely different memories are overlooked.

It seems wholly illogical to transfer structural and operational details of the semiconductor SRAM of Clemons to the active matrix-addressable ferroelectric memory of Kuroda and certainly such an undertaking would not yield the present invention, which specifically is concerned with both limiting the number of sense amplifiers and obtaining a suitable high data rate by an appropriate segmenting of a word line and providing for reading each word line segment in parallel by using a sense amplifier block with the number of sense amplifiers equal to the number of bit lines defining a word line segment in order that a high data rate may be maintained and the number of sense amplifiers kept to manageable proportions, whereas the number of bit lines of the memory according to the present invention can be as large as desired.

Thus, Kuroda in combination with Clemons fails to teach, *inter alia,* each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment, as recited in claims 1, 12 and 13.

Dependent Claims (Seyyedi & Dierke)

Regarding the dependent claims and the additional cited prior art it should be noted that US 5,969,380 (Seyyedi) does not teach more than volumetric ferroelectric memory although this particular architecture has been disclosed by the Japanese company Olympus back around 1986. The novelty of Seyyedi of course does not lie in the volumetric architecture, but rather in the use of an insulating material between the rows of conductors to reduce crosstalk.

In regard of US 5,734,615 (Dierke) it is not concerned with a ferroelectric memory at all, but rather a memory testing apparatus. The use of multiplexers in this particular testing device is almost the opposite of that in the present invention or similar types of memory which would have

as their goal to simplify the output and data-sensing arrangements. In Dierke it is explicitly stated that when memories have parallel outputs wider than one byte of data, multiplexers are provided for successively applying the data from the memories to the output unit one byte at a time, and this can hardly be equated with parallel read in the sense of the present invention, e.g. reading 128 bytes in parallel.

Response to Examiner's Comments

Some of the comments made by the Examiner do not make much sense to Applicants. For instance on page 5, bottom section, the Examiner states that "it would have been obvious at the time of the invention was made etc.... to substitute a multiplexing means of Dierke for the multiplexing means of Clemons, since both means are equivalent for simultaneously connecting bit lines of a segment with an associated sensing means etc." This is not true as Dierke teaches how to reduce the output to one byte at a time, while Clemons' explicit goal is to allow a simultaneous output in a so-called byte block arrangement of 8 bits constituting a byte.

Also, Clemons which was granted as a patent on 8 July 1986 which predates the priority date of Kuroda by 6 years. The Examiner states that "the invention of Clemons wass discloses as an improvement over the 'prior art' embodiment in Fig. 1 of Clemons, which is similar to that of Kuroda." Applicant's don't follow the Examiner's reasoning with this statement, i.e., the memory device similar to that of Kuroda is regarded as prior art by Clemons. If that were the case, with Clemons having a priority date six (6) years earlier than Kuroda, it would be hard to understand why the Kuroda patent was granted at all.

Further Clemons prior art, fig. 1 can not be equated with the memory device of Kuroda. It should be noted that no prior art cited in Clemons is reiterated or can be found in Kuroda – understandably as Clemons and Kuroda concern two entirely different memory devices. The claim that the prior art embodiment in fig. 1 of Clemons is similar to that of Kuroda is anyway flawed, as Kuroda is a kind of semi-active ferroelectric memory with the explicit goal to achieve a higher integration by reducing the number of switching

element and at the same time obtain an extremely low voltage stress ratio by being able to limiting the voltage disturb in a ferroelectric memory to a memory circuit of only 8 memory cells. Nothing of this sort can of course be read into the prior art embodiment of fig. 1 in Clemons.

Finally, as shown above, it would by no means have been obvious combining one sort of memory with a completely different sort of memory to achieve the improvement of the present invention, albeit at the cost of destroying the improvement in regard of other aspects of ferroelectric memories, such as the explicit goal of the cited prior art memory of Kuroda. And it should be noted that neither the latter nor the present invention is concerned with a bytewise memory organization. The data organization in the device of the present invention depends on how its logical address space is configured and this can be done without the restrictions that a device according to either Clemons or Kuroda would impose.

Thus, applicants respectfully submit that the problem remains with the combination of Kuroda and Clemons as discussed above. Therefore, the combination of Kuroda and Clemons fails to teach or suggest each and every feature of claims 1, 12 and 13 as required.

Further, Dierke and Seyyedy fail to remedy the deficiencies of Kuroda and Clemons. Accordingly, applicants respectfully submit that neither Kuroda, Clemons, Dierke or Seyyedy alone or in combination teach or suggest the above claimed limitations. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

CONCLUSION

In view of the above amendment, applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. Billings Reg. No. 48,917 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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